DN90

ZXGD3101 Synchronous MOSFET controller improves energy efficiency of dual-output power supply

Yong Ang, Applications Engineer, Diodes Incorporated

Introduction

This design note addresses the challenge of applying Synchronous Rectification on dual-outputs Flyback converter. It discusses the active mode efficiency improvement with the aid of the ZXGD3101 synchronous MOSFET controller and studies its practical limit against normal rectification method. Finally, experimental verification is presented to demonstrate the performance improvement in a 40W LCD monitor power supply.

Synchronous Rectifier configuration in a dual-output power supply

A common technique to construct transformer for multiple output power supply is to stack the secondary windings with the same polarity and share a common ground instead of having separate windings, as shown in Figure 1. This is particularly conducive to maximizing regulation in applications such as LCD monitor SMPS. Typically, LCD monitors require a 5V output for the microprocessor as well as a 12V output to supply the LCD backlight inverter. While the '+5V' output is the main regulated output using a voltage reference, the regulation of the quasi-regulated '+12V' output is improved through the stacked winding.

Furthermore, the winding for the '+5V' output will provide the return to ground and forms part of the winding for the '+12V' output. This has the merits of keeping the total number of secondary turns low and improves cross regulation of the multiple outputs. The wire size for the '+5V' winding needs to be chosen to accommodate its own maximum load current plus the output current of the '+12V' output stacked on top of it.

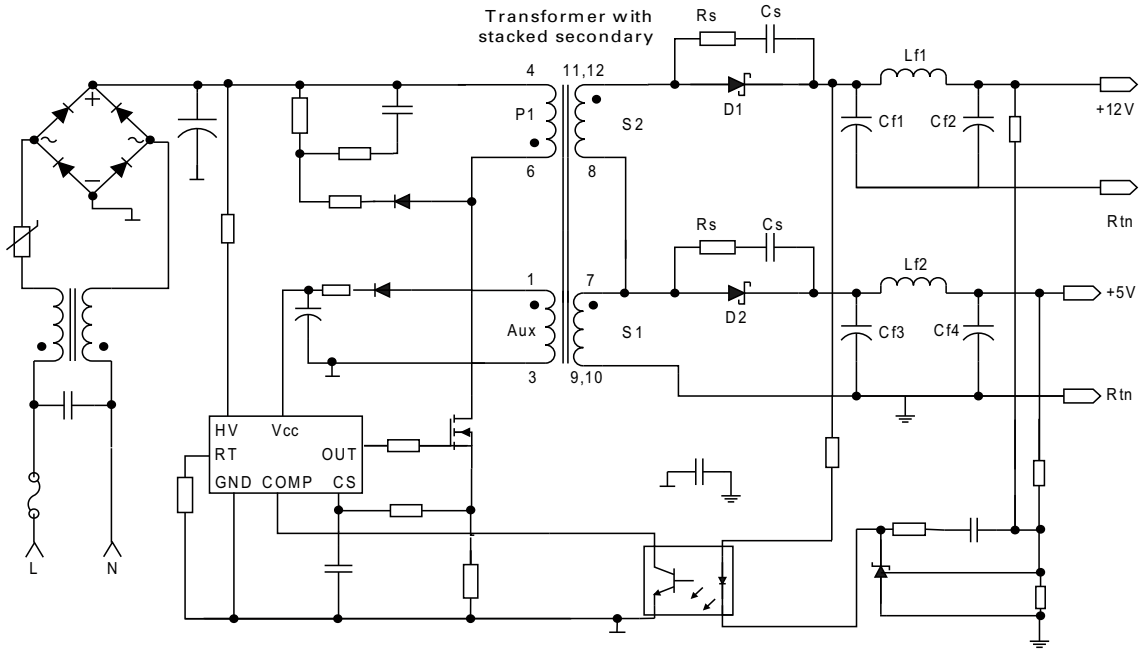


Figure 1 - Dual-output power supply with Schottky diodes

Nevertheless, the previously stacked winding approach does not lend itself readily to implementation of synchronous rectification on both outputs. Contrary to the separated secondary approach where a common MOSFET source connection is available on the ground return, negative side synchronous rectification cannot be implemented for stacked winding. Positive side rectification on both outputs is less attractive due to extra BOM cost and count as it prohibits a common synchronous rectifier drive circuit.

A new configuration is described here which enables two MOSFETs to be driven from a common ZXGD3101 synchronous MOSFET controller. As shown in figure 2, the proposed configuration has the synchronous rectifier 'Control' block positioned on the lower node of the stacked up winding, where it is also connected to the top node of the 5V output winding. A single controller can now detect the body diode conduction of the 'Control' MOSFET and outputs a gate drive voltage proportional to the voltage drop across this MOSFET. The same gate voltage is used to drive the second MOSFET on the '+5V' output, 'synchronous' MOSFET, though the gate voltage level is independent of the current status in the 'synchronous' MOSFET. It is also important to note that as the ZXGD3101's 2.5A source and sink current is now shared by two MOSFETs, the likelihood of shoot through current occuring will increase if a very high gate charge MOSFET is used. A snubber network compromising of Cs and Rs should be included to suppress transformer leakage inductance induced drain voltage oscillations and reduce EMI emissions.

The recommended supply voltage to 'V_{CC}' pin on the ZXGD3101 is 8 to 10V to ensure sufficient gate voltage to fully enhance the synchronous MOSFETs. Due to the ease of connection, the supply voltage was derived directly from the '+12V' output via an emitter-follower transistor. The 'collector' pin of Q1, FMMT491A should be connected to the left hand side of the output EMI filter inductor to minimize coupled noises to the output. Nevertheless, there is downside to such a configuration which will be explained later and an alternative configuration will be proposed.

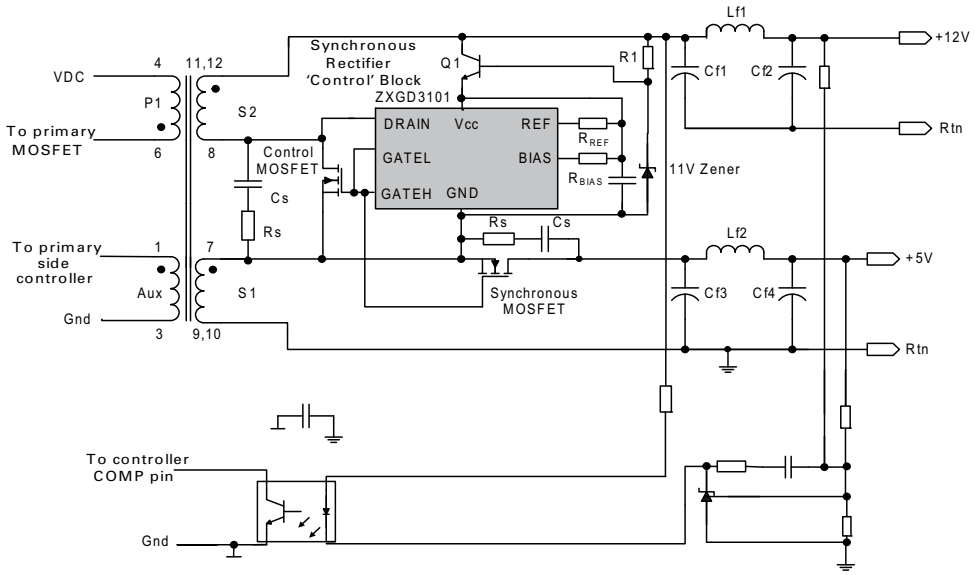


Figure 2 - Proposed configuration of ZXGD3101 in a dual-output Flyback SMPS

Efficiency test

Laboratory evaluation is conducted on a Flyback converter to assess the performance benefits of Synchronous Rectification over Schottky diodes. The converter is built around a PWM based primary side controller operating at 63kHz to obtain two output voltages. The '+5V' and '+12V' output can supply a maximum load current of 2.5A and 2A respectively. Table 1 shows the efficiency measurement with MBR30100CT as output rectifier diodes. The average active mode efficiency of the SMPS is 86.62% at 100Vac input.

To achieve a significant efficiency improvement, considering the level of RMS current, a MOSFET with an on-resistance below 20mΩ was selected. Thus a 16mΩ, 79A, 82nC MOSFET is selected so that the voltage-drop across the Drain-Source pins is within 50 to 100mV at the peak of the secondary-side current. The turn-off threshold voltage of the controller was set to '-20mV' to minimize/prevent reverse Drain current flow. For more information about selecting the turn-off threshold voltage refer to the device datasheet. As shown in Table 2, synchronous rectification can indeed achieve a significant efficiency improvement over MBR10100CT across a load range at both 100Vac and 240Vac input. At 100Vac, the circuit is 1.4% more efficiency against the Schottky diode at 50% loading and has 3.2% better efficiency at 100% loading.

Table 1- Active mode efficiency measurement (MBR10100CT)

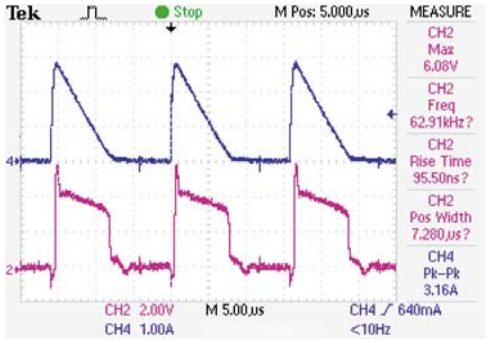
Loading (%)	Vin	Pin (W)	V_{+5V}	I_{+5V}	V_{+12}	I_{+12}	Po (W)	Eff (%)
25	100	13.36	5.058	0.5	11.97	0.75	11.49	85.99
50	100	23.16	5.049	1.0	12.05	1.25	20.11	86.83
75	100	36.47	5.043	1.5	12.09	1.99	31.73	87.01
100	100	46.61	5.033	1.99	12.14	2.50	40.38	86.65
Average efficiency (%)								86.62
Loading (%)	**Vin**	**Pin (W)**	**V_{+5V}**	**I_{+5V}**	**V_{+12}**	**I_{+12}**	**Po (W)**	**Eff (%)**
25	240	13.94	5.057	0.5	11.97	0.75	11.51	82.52
50	240	23.81	5.05	1.0	12.04	1.25	20.10	84.42
75	240	36.96	5.049	1.5	12.05	2.01	31.65	85.62
100	240	47.05	5.043	1.99	12.09	2.5	40.29	85.64
Average efficiency (%)								84.55

Table 2 – Active mode efficiency measurement (Synchronous Rectification)

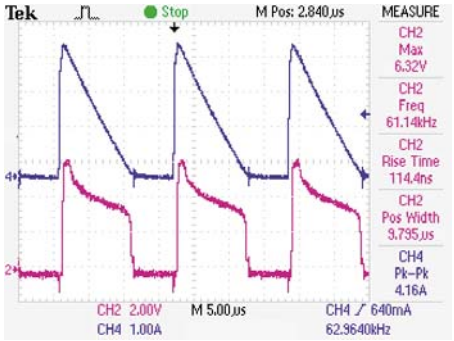
Loading (%)	Vin	Pin (W)	V_{+5V}	I_{+5}	V_{+12}	I_{+12}	Po (W)	Eff (%)
25	100	12.99	5.097	0.5	11.62	0.75	11.27	86.76
50	100	22.24	5.097	1.0	11.63	1.24	19.63	88.27
75	100	34.46	5.098	1.5	11.61	2.02	30.87	89.55
100	100	43.71	5.096	2.0	11.63	2.50	39.27	89.82
Average efficiency (%)								88.60
Loading (%)	**Vin**	**Pin (W)**	**V_{+5V}**	**I_{+5}**	**V_{+12}**	**I_{+12}**	**Po (W)**	**Eff (%)**
25	240	13.24	5.097	0.5	11.61	0.75	11.25	84.97
50	240	22.47	5.097	1	11.63	1.25	19.64	87.41
75	240	35.03	5.101	1.5	11.61	2.00	30.88	88.15
100	240	44.32	5.099	2	11.61	2.47	39.18	88.38
Average efficiency (%)								87.22

Figure 3(a) to (d) show the operating waveforms on the 'Control' MOSFET as the circuit traverses from Continuous Conduction (CCM) into Discontinuous Conduction (DCM) Mode operation with decreasing loads. In Figure 3(d), the Gate voltage reaches 8.5V when the MOSFET current was high to obtain a low resistance at 100% loading. The gate enhancement then eases off gradually

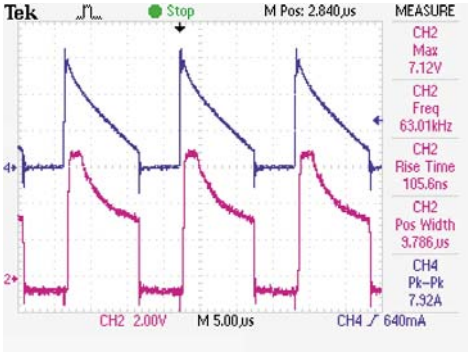
as the Drain current through the MOSFET decreases, ensuring a quick turn-off of the synchronous MOSFETs upon primary MOSFET turn-on.



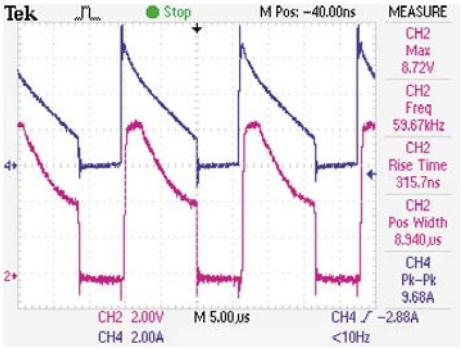
(a) 25% loading



(b) 50% loading



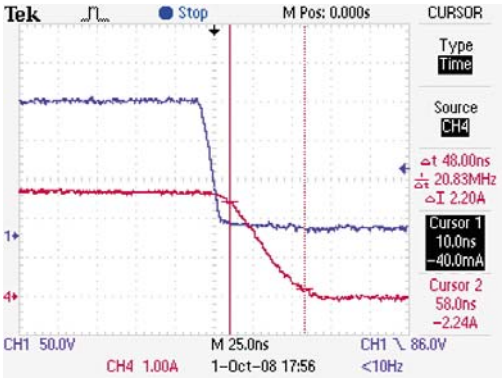
(c) 75% loading



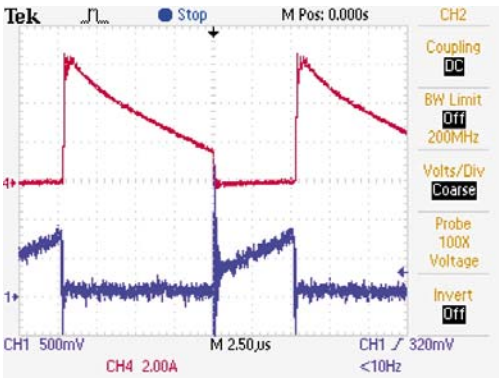
(d) 100% loading

Figure 3 - Synchronous rectifier operating waveform (CH2: Gate voltage; CH4: Drain current)

At turn off, the synchronous MOSFETs currents are pulled down rapidly as the primary MOSFET current rises. This forces the Drain-Source voltage across the 'Control' MOSFET to drop beyond the turn-off threshold and the ZXGD3101 drives the gate off. As the secondary winding current fall time is limited to 48ns by the winding leakage inductance (see Figure 4), the controller drives off both the 'Control' and 'Synchronous' MOSFET safely and minimizes the possibility of cross conduction.



(a)
CH1: Primary switch drain voltage;
CH4: 'Control' MOSFET current



(b)
CH1: Primary switch current sense voltage;
CH4: 'Control' MOSFET current

Figure 4 - Synchronous MOSFET turn-off in CCM

In Figure 3(b) and (c), the proportional gate drive scheme reduces the gate voltage magnitude when a lower current flows through the MOSFET at 50% and 75% loading. Although this produces a larger on-state resistance, the subsequent increase in conduction voltage drop will ensure that the controller can hold up the gate voltage above 2-3V until the point where the current reaches zero. This negative feedback mechanism helps to prevent the MOSFETs from been turned off prematurely.

At 25% loading, the MOSFET current decreases linearly (see Figure 3(a)); the MOSFET is driven off at the zero current point to ensures there is no reverse current flow.

Other design considerations

Efficiency results in the previous section show that synchronous rectification can yield more than 3% better efficiency than diodes in the 40W dual-output power supply under certain load and input voltage combinations. This improvement is attributed to the significant conduction loss saving from the MOSFETs.

The on-state conduction loss could potentially be further reduced if a lower on-state resistance MOSFET is used as either/both 'Control' and 'Synchronous' MOSFET. However care has to be taken when a very low resistance is used as the subsequent on-state voltage drop across Source-Drain may not be sufficient to induce the ZXGD3101 to output a high enough gate voltage. This forms a negative feedback loop consisting of the MOSFET and the controller which would cause the gate voltage to go into sustained oscillation. Under such circumstances, the full capability of the MOSFET could not be utilized and results in a non-appreciable efficiency improvement compared with a higher resistance MOSFET. Therefore, it is difficult to obtain even greater efficiency without some serious design compromises and modifications.

At low load conditions, generally a power supply within an LCD monitor will have to meet the 'sleep' or 'off-mode' power requirement of less than 1W. Although the display unit consumes minimal power in this mode, the power supply still has to supply a finite amount of power especially to the '+5V' output. Figure 5 below shows the available output power vs. line voltage for an input power of 1W.

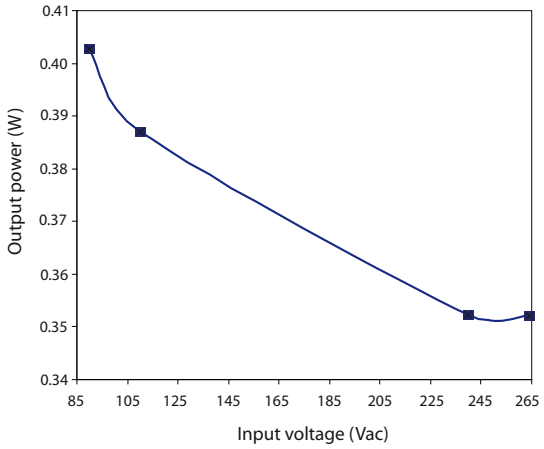


Figure 5 Available power on '+5V' output to achieve 1W sleep mode input power

Another interesting observation is that the circuit will have a high no load power consumption with synchronous rectification as shown in Table 3. The no load power consumption will be higher than that with Schottky diode rectification. The increased no load power is due to the accumulation of losses associated with gate charge loss, power consumption of the ZXGD3101 and its supply circuit. As the Vcc supply is derived directly from the '+12V' output through an emitter follower transistor Q1, as shown in Figure 2, Q1 blocks the differential ac voltage at '+12V'

output pin relative to the 'Control' MOSFET source pin. This incurs extra power dissipation within the transistor.

Table 3

Vin (Vac)	Pin (W)
100	0.44
240	0.42
264	0.46

Although this is far out-weighted by the significant conduction loss saving provided by synchronous rectification in active mode, the no load consumption could be reduced by augmenting an additional supply winding for the controller similar to that shown in Figure 5. This necessitates a slight modification to the existing transformer design where the number of turns for the additional winding is chosen so that voltage at C1 relative to the common MOSFET source node is a dc voltage of less than 12V. D1 is a low power rectifier diode of 100mA rating whilst the value of R1 is chosen to be 10kΩ to keep the power dissipation low. This significantly minimizes the voltage drop across Q1 so that the no load and sleep mode power consumption of the power supply could be further reduced.

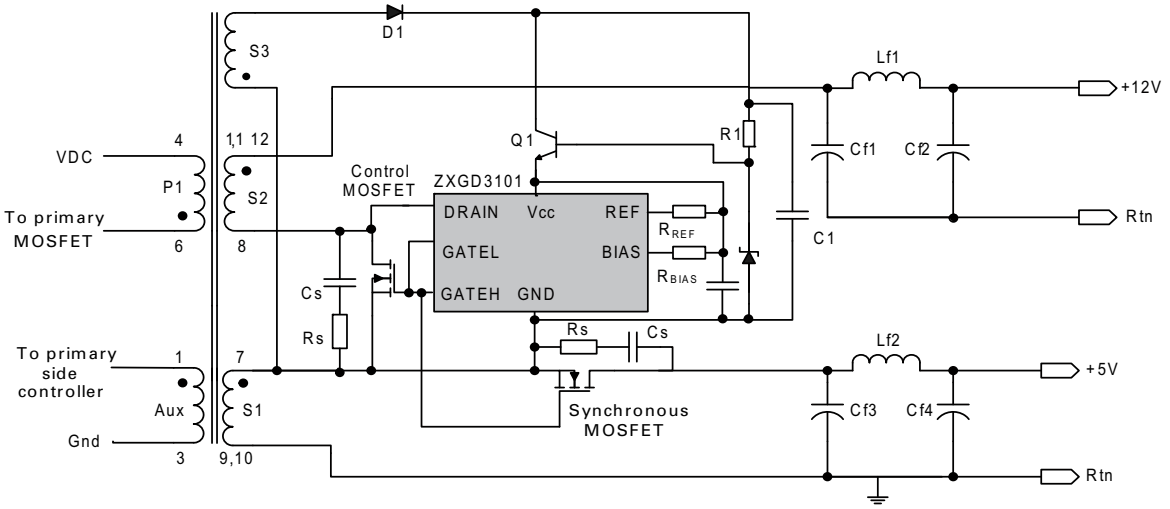


Figure 6 - Alternative winding configuration reduces no load and sleep mode power consumption

Another important aspect to be considered is the synchronous rectification on the power supply cross regulation performance. Table 4 (following page) shows the data for the outputs under various loading conditions at 100 and 264Vac. The regulation on the more critical '+5V' output was within ±5% under the considered conditions.

Table 4 – Cross regulation matrix

Output		V_{+5V}		V_{+12V}	
I_{+5V}	I_{+12V}	100Vac	264Vac	100Vac	264Vac
0	0	5.053	5.063	12.01	11.91
0.4	2.5	5.115	5.117	11.42	11.44
2	0.5	5.017	5.014	12.31	12.33
2	2.5	5.093	5.1	11.63	11.61

Conclusion

A novel configuration of synchronous rectification on a dual-output Flyback converter has been proposed that enables two MOSFETs to be driven by a single ZXGD3101 synchronous MOSFET controller. This enables the power supply to achieve excellent performance both in term of active mode and sleep mode power efficiency. The main control loop is closed around the '+5V' output and the '+12V' output was configured as a stacked winding to ensure a manageable transformer design as well as improving cross regulation performance.

Definitions

Product change

Diodes Incorporated reserves the right to alter, without notice, specifications, design, price or conditions of supply of any product or service. Customers are solely responsible for obtaining the latest relevant information before placing orders.

Applications disclaimer

The circuits in this design/application note are offered as design ideas. It is the responsibility of the user to ensure that the circuit is fit for the user's application and meets with the user's requirements. No representation or warranty is given and no liability whatsoever is assumed by Diodes Inc. with respect to the accuracy or use of such information, or infringement of patents or other intellectual property rights arising from such use or otherwise. Diodes Inc. does not assume any legal responsibility or will not be held legally liable (whether in contract, tort (including negligence), breach of statutory duty, restriction or otherwise) for any damages, loss of profit, business, contract, opportunity or consequential loss in the use of these circuit applications, under any circumstances.

Life support

Diodes Zetex products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:
   1. are intended to implant into the body

or

   2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labelling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Reproduction

The product specifications contained in this publication are issued to provide outline information only which (unless agreed by the company in writing) may not be used, applied or reproduced for any purpose or form part of any order or contract or be regarded as a representation relating to the products or services concerned.

Terms and Conditions

All products are sold subjects to Diodes Inc. terms and conditions of sale, and this disclaimer (save in the event of a conflict between the two when the terms of the contract shall prevail) according to region, supplied at the time of order acknowledgement.

For the latest information on technology, delivery terms and conditions and prices, please contact your nearest Diodes sales office .

Quality of product

Diodes Zetex Semiconductors Limited is an ISO 9001 and TS16949 certified semiconductor manufacturer.

To ensure quality of service and products we strongly advise the purchase of parts directly from Diodes Incorportaed or one of our regionally authorized distributors. For a complete listing of authorized distributors please visit: **www.diodes.com** or **www.zetex.com**

Diodes Zetex Semiconductors does not warrant or accept any liability whatsoever in respect of any parts purchased through unauthorized sales channels.

ESD (Electrostatic discharge)

Semiconductor devices are susceptible to damage by ESD. Suitable precautions should be taken when handling and transporting devices. The possible damage to devices depends on the circumstances of the handling and transporting, and the nature of the device. The extent of damage can vary from immediate functional or parametric malfunction to degradation of function or performance in use over time. Devices suspected of being affected should be replaced.

Green compliance

Diodes Zetex Semiconductors is committed to environmental excellence in all aspects of its operations which includes meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.

All Diodes Zetex components are compliant with the RoHS directive, and through this it is supporting its customers in their compliance with WEEE and ELV directives.

Product status key:

"Preview"	Future device intended for production at some point. Samples may be available
"Active"	Product status recommended for new designs
"Last time buy (LTB)"	Device will be discontinued and last time buy period and delivery is in effect
"Not recommended for new designs"	Device is still in production to support existing designs and production
"Obsolete"	Production has been discontinued

Datasheet status key:

"Draft version"	This term denotes a very early datasheet version and contains highly provisional information, which may change in any manner without notice.
"Provisional version"	This term denotes a pre-release datasheet. It provides a clear indication of anticipated performance. However, changes to the test conditions and specifications may occur, at any time and without notice.
"Issue"	This term denotes an issued datasheet containing finalized specifications. However, changes to specifications may occur, at any time and without notice.

Sales offices

The Americas

3050 E. Hillcrest Drive
Westlake Village,
CA 91362-3154
Tel: (+1) 805 446 4800
Fax: (+1) 805 446 4850

Europe

Kustermann-Park
Balanstraße 59,
D-81541 München
Germany
Tel: (+49) 894 549 490
Fax: (+49) 894 549 4949

Taiwan

7F, No. 50,
Min Chuan Road
Hsin-Tien
Taipei, Taiwan
Tel: (+886) 289 146 000
Fax: (+886) 289 146 639

Shanghai

Rm. 606, No.1158
Changning Road
Shanghai, China
Tel: (+86) 215 241 4882
Fax (+86) 215 241 4891

Shenzhen

ANLIAN Plaza, #4018
Jintian Road
Futian CBD,
Shenzhen, China
Tel: (+86) 755 882 849 88
Fax: (+86) 755 882 849 99

Korea

6 Floor, Changhwa B/D,
1005-5 Yeongtong-dong,
Yeongtong-gu, Suwon-si,
Gyeonggi-do, Korea 443-813
Tel: (+82) 312 731 884
Fax: (+82) 312 731 885